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L15: Entry 17 of 18

File: USPT

Mar 10, 1998

US-PAT-NO: 5727227

DOCUMENT-IDENTIFIER: US 5727227 A

TITLE: Interrupt coprocessor configured to process interrupts in a computer system

DATE-ISSUED: March 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Schmidt; Rodney W.	Austin	TX		
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ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices	Sunnyvale	CA			02

APPL-NO: 08/ 559659 [\[PALM\]](#)

DATE FILED: November 20, 1995

INT-CL: [06] [G06](#) [F](#) [1/00](#)

US-CL-ISSUED: 395/800; 395/733, 364/228.6, 364/DIG.1

US-CL-CURRENT: [712/36](#); [710/260](#)

FIELD-OF-SEARCH: 395/800, 395/733, 395/737, 364/228.6, 364/DIG.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	H1385	December 1994	Stickel et al.	395/800
<input type="checkbox"/>	5155839	October 1992	Weppler	395/500
<input type="checkbox"/>	5193189	March 1993	Flood et al.	395/673
<input type="checkbox"/>	5603035	February 1997	Erramoun et al.	395/733

OTHER PUBLICATIONS

Intel Corp., "MultiProcessor Specification", Version 1.1 Apr., 1994, pp. 1.1-Glossary 2.

Hummel, "PC Magazine Programmer's Technical Reference: The Processor and

Coprocessor", 1992, pp. 153-182.

Intel Corp., "Microprocessor & Peripheral Handbook-vol. I Microprocessor", 1989 pp. 2-259 through 2-277.

Singh et al., "16-Bit and 32-Bit Microprocessors Architecture, Software, and Interfacing Techniques", 1991, pp. 302-305.

ART-UNIT: 232

PRIMARY-EXAMINER: Harrity; John E.

ATTY-AGENT-FIRM: Conley, Rose & Tayon Kivlin; B. Noel

ABSTRACT:

A computer system employing an interrupt coprocessor is provided. The interrupt coprocessor is signaled by an interrupt controller to service a particular interrupt request. The interrupt coprocessor may include limited functionality, such that if a particular interrupt request is beyond the capabilities of the interrupt coprocessor, the microprocessor is interrupted. Context saves may be avoided in the interrupt coprocessor. Interrupt latency is reduced, as well as interruption of one or more main microprocessors in the computer system. Several embodiments are shown with a range of interrupt servicing capabilities. A data pump is shown, which is configured to transfer data from a source to a destination. A microcontroller is shown, which may manipulate the data as it is moved from source to destination or access the interrupting device to determine the service needed. Finally, a microprocessor similar to the main microprocessors of the computer system is shown. The microprocessor is capable of accessing system resources in a similar fashion to the main microprocessor, and therefore is capable of performing all interrupt servicing functions.

27 Claims, 4 Drawing figures

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Detailed Description Text (18):

In order to allow more flexibility in programming interrupt service routines, the Compare and Branch instructions are provided. The Compare instruction compares two values from among the values stored in data buffer 46, source register 48, destination register 50, and an immediate value provided with the instruction. The result of the compare is a set of bits indicative of the first value being greater than the second value, the first value being less than the second value, and the first value being equal to the second value. The Branch instruction is configured to branch to an address indicated by an immediate value provided with the instruction if a selected one of the set of bits described above is set or clear. As with the Loop instruction, the immediate value provided with the Branch instruction is a relative offset which is added to the address of the Branch instruction to determine the target of the branch.